

FIG. 1

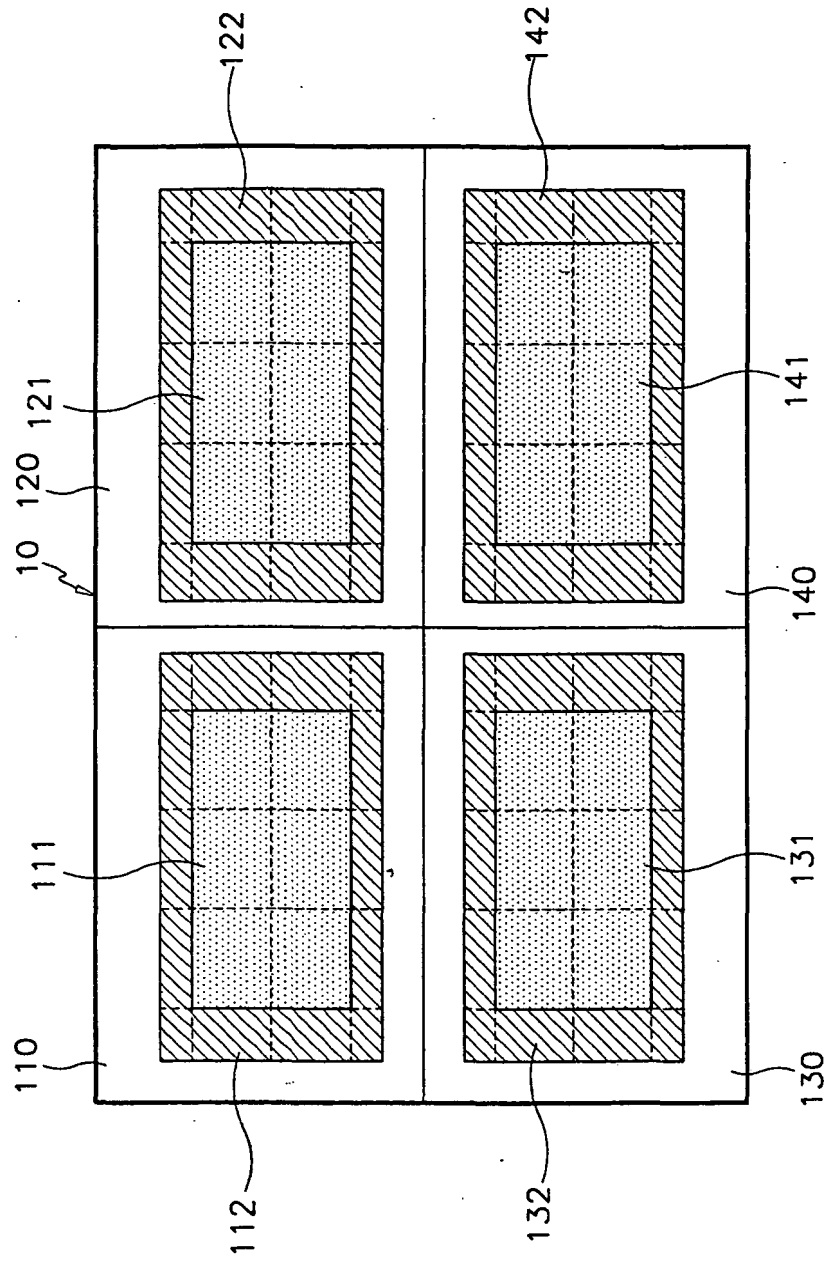


FIG.2

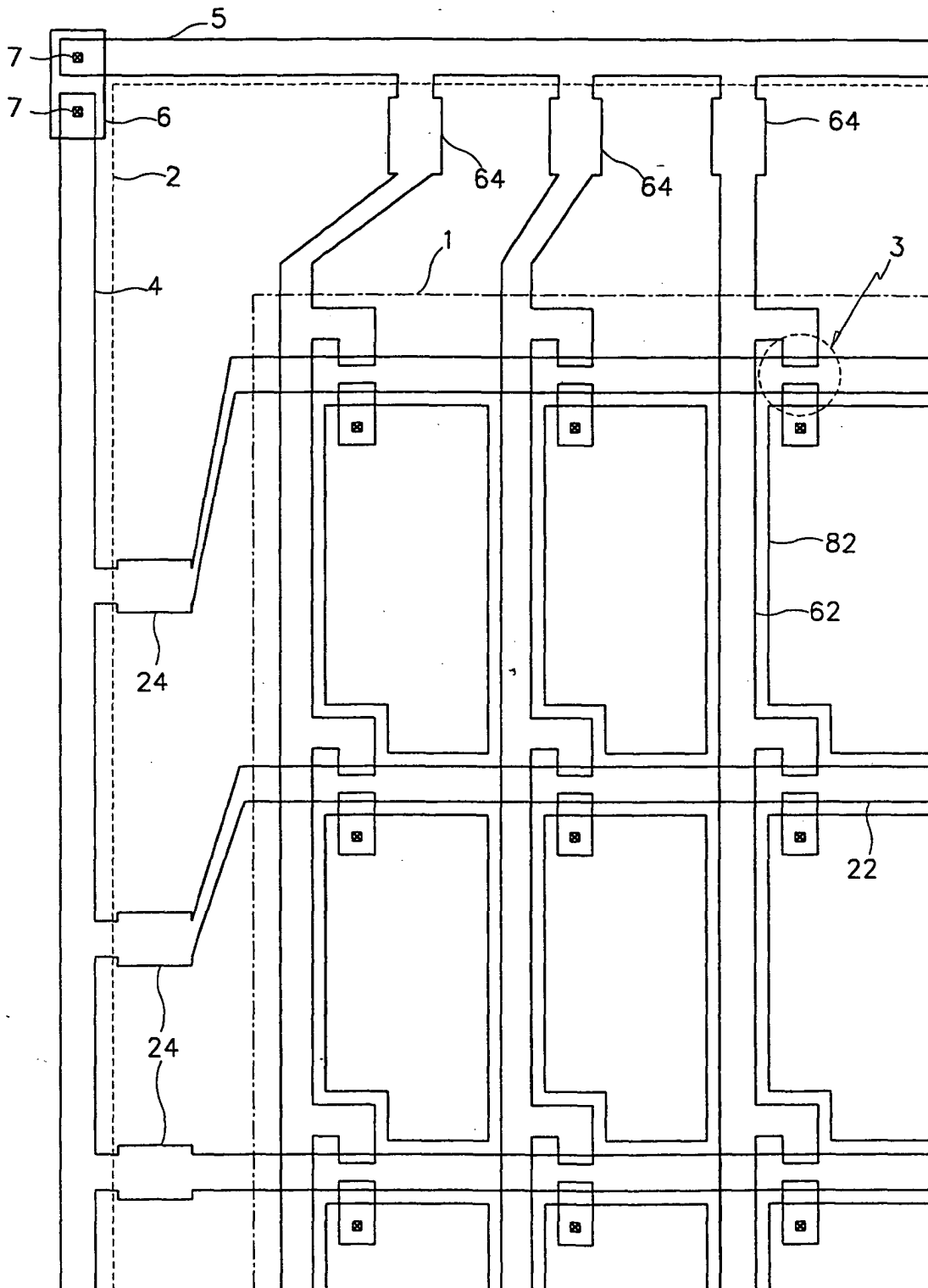


FIG.3

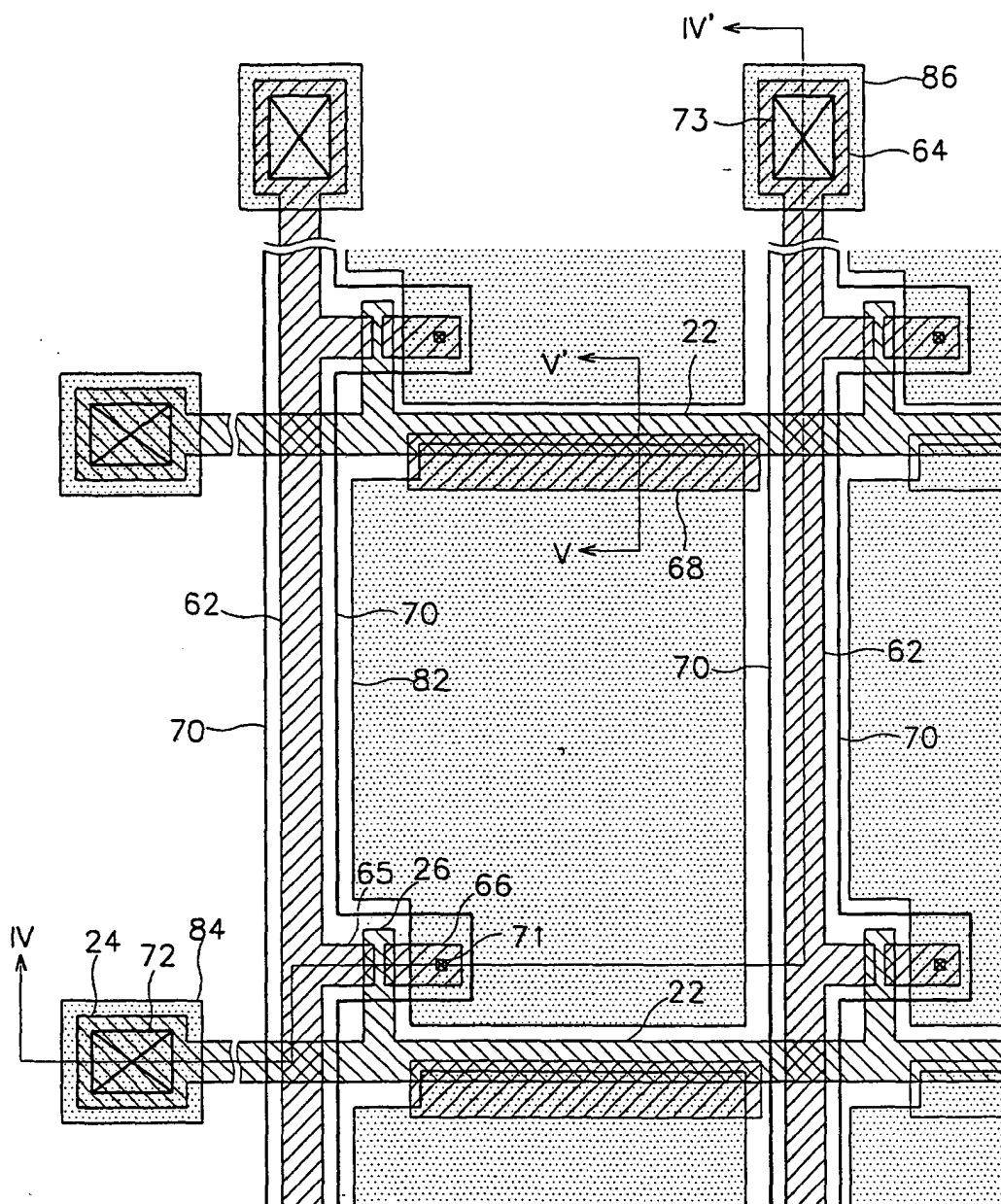


FIG. 4

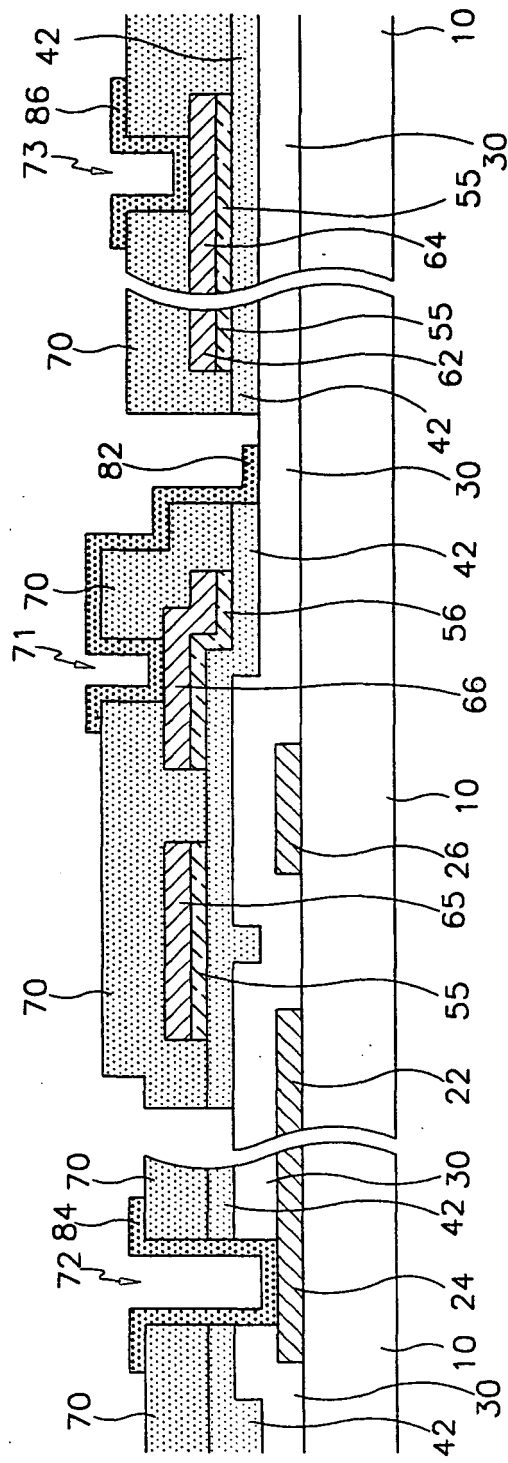


FIG. 5

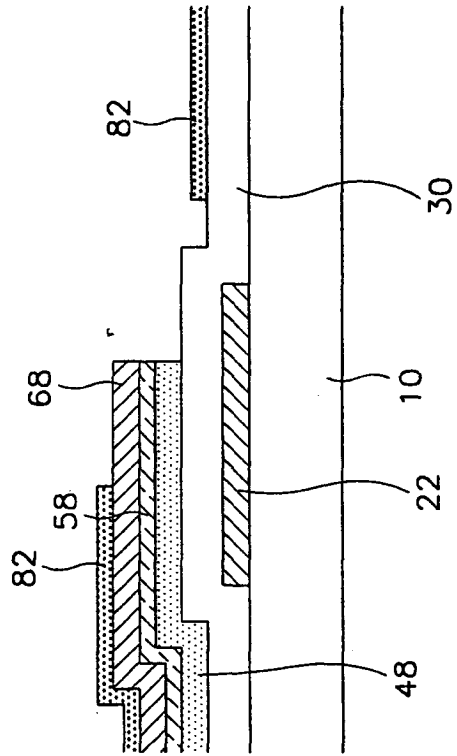


FIG. 6A

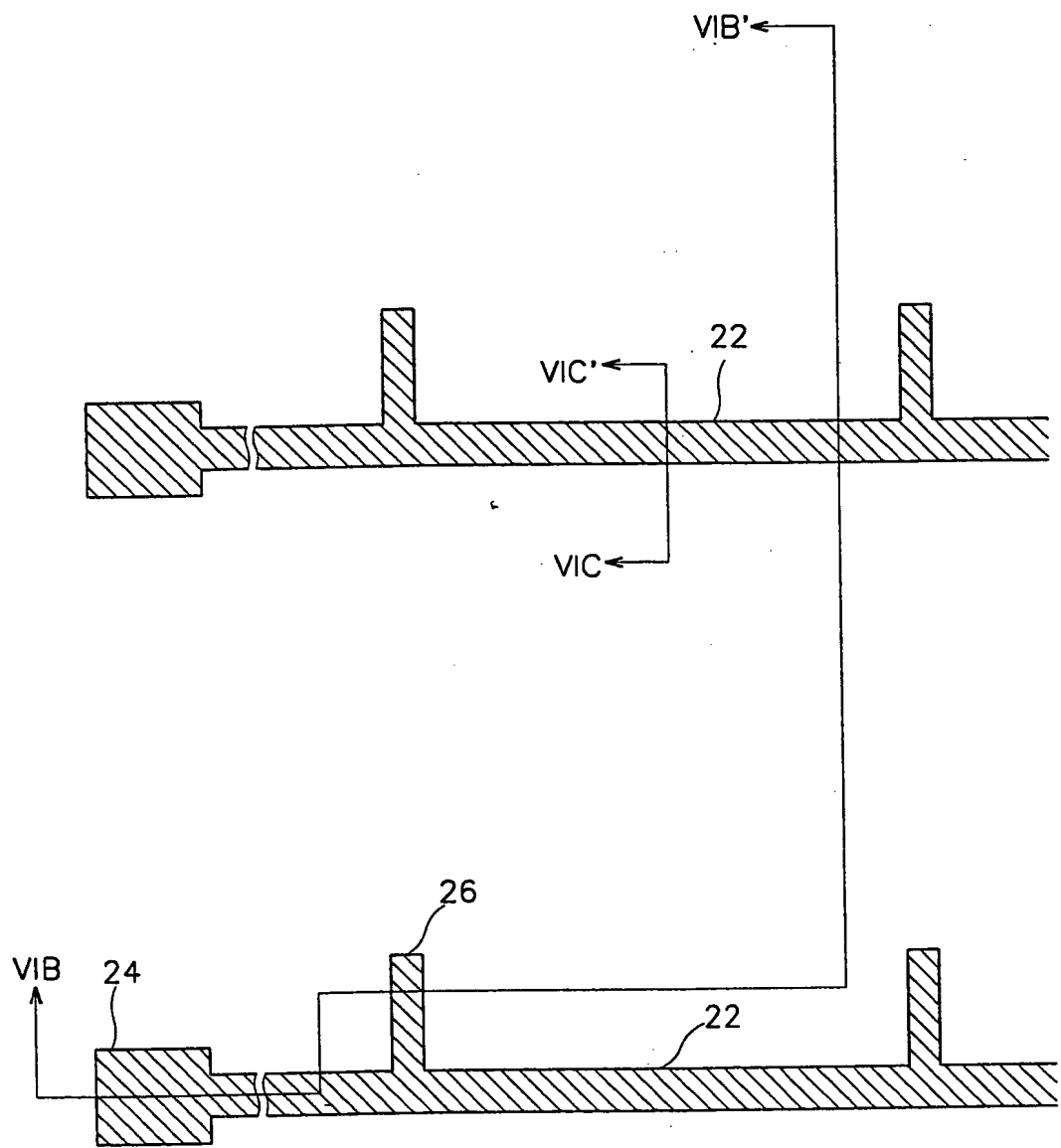


FIG. 6B

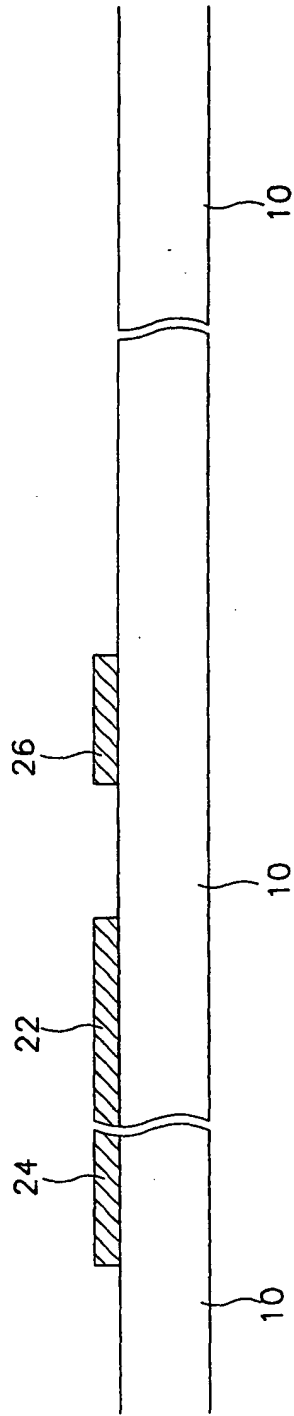


FIG. 6C

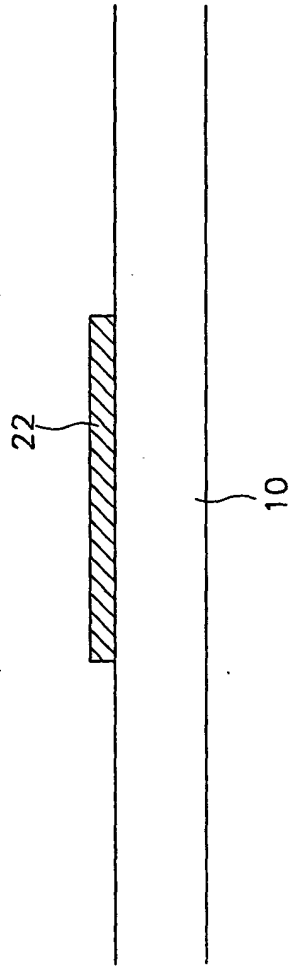


FIG.7A

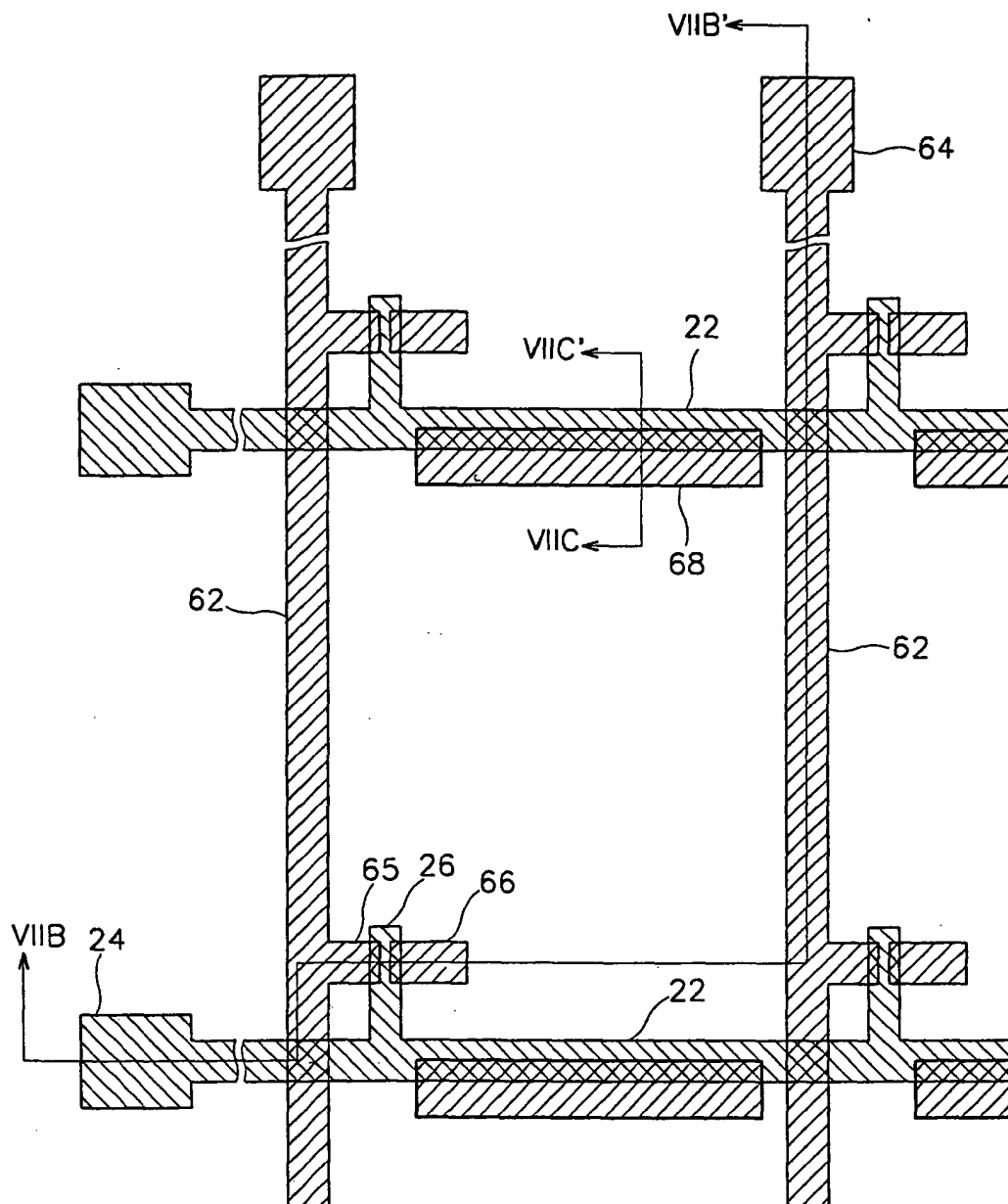


FIG. 7B

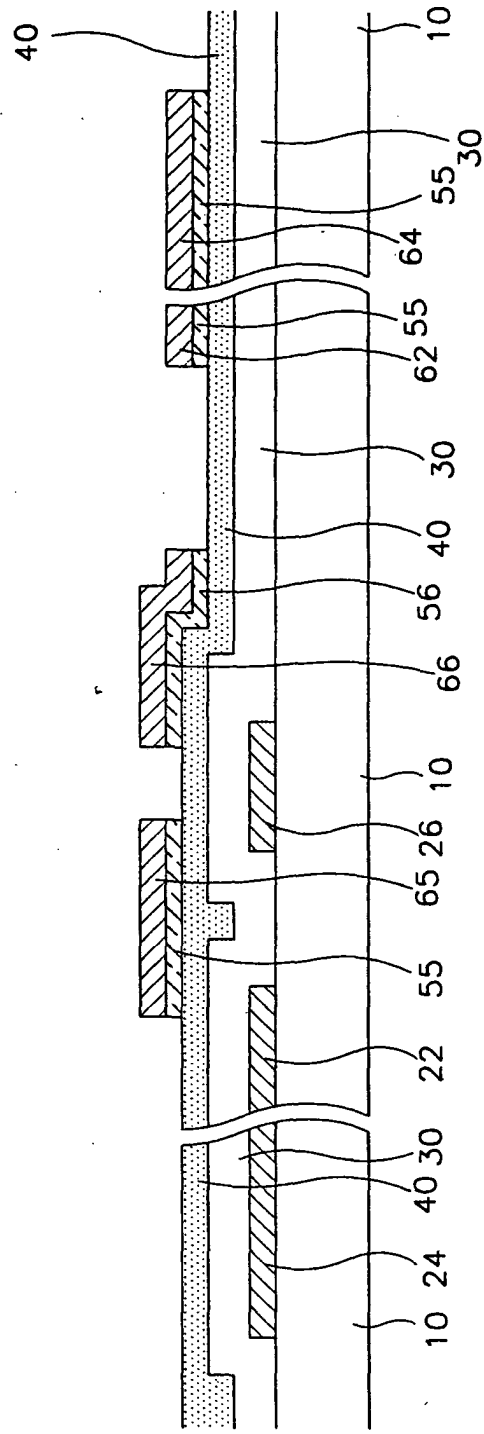


FIG.7C

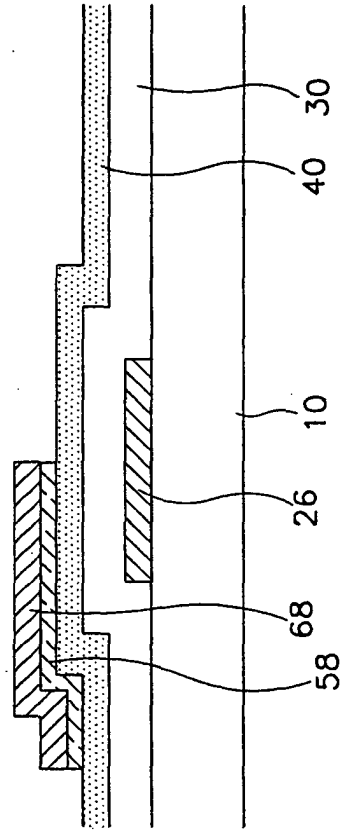


FIG.8A

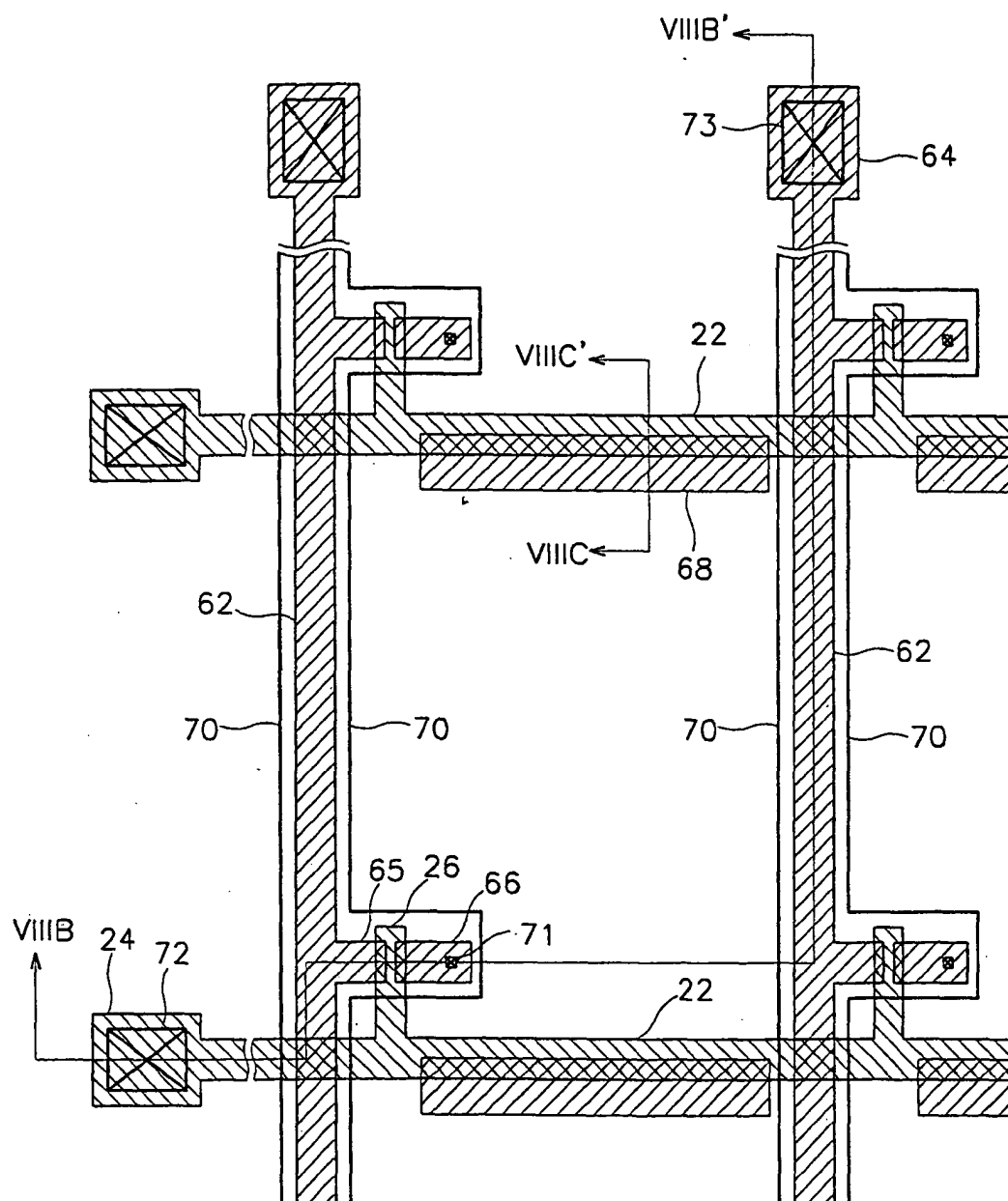


FIG. 8B

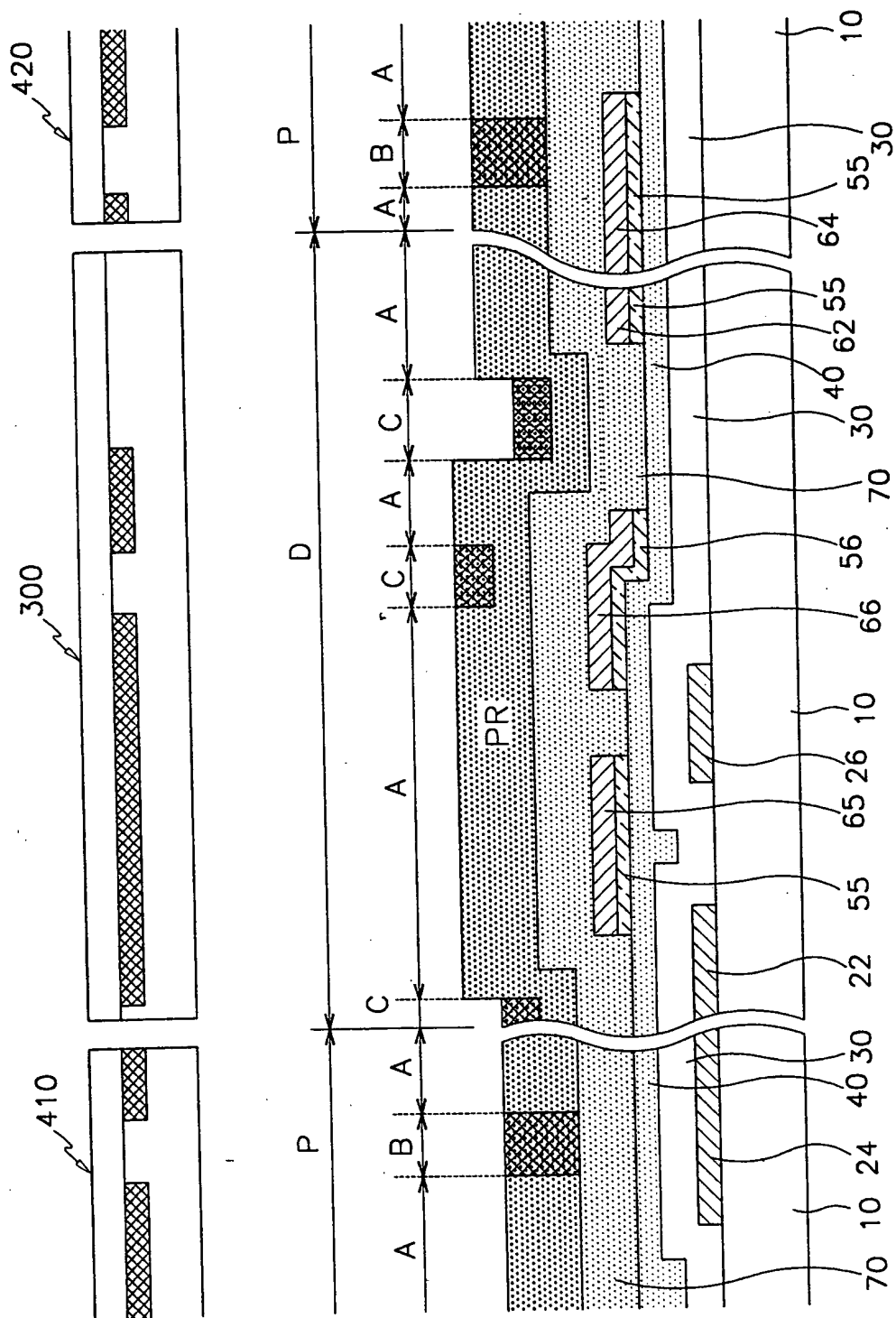


FIG.8C

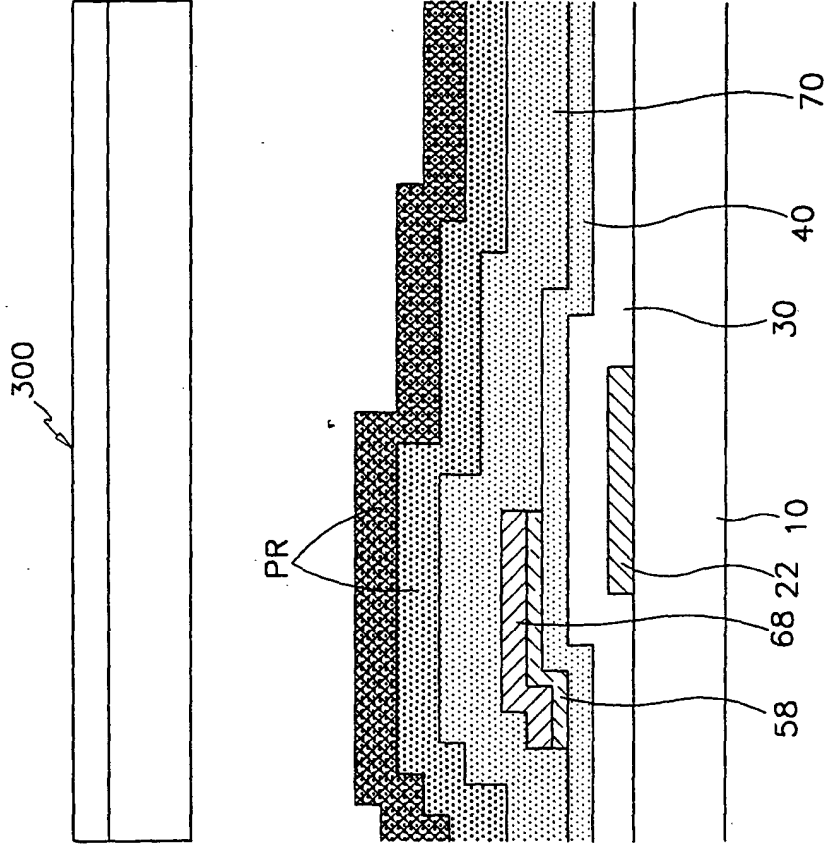


FIG.9A

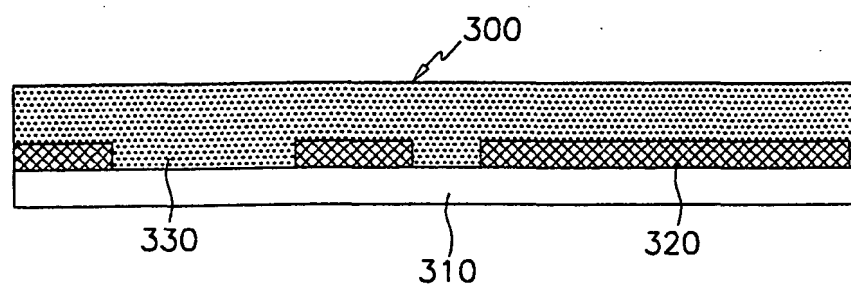


FIG.9B

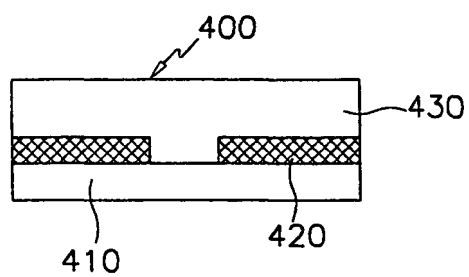


FIG.10A

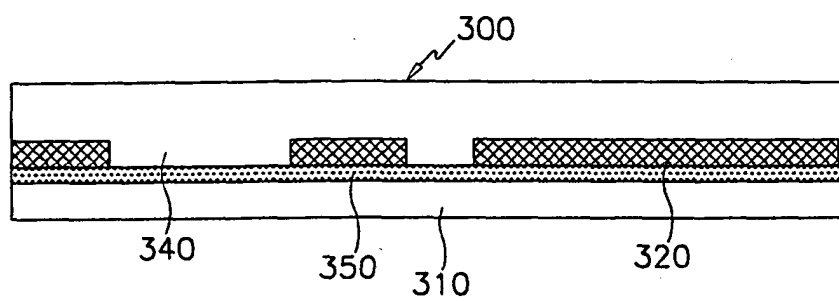


FIG.10B

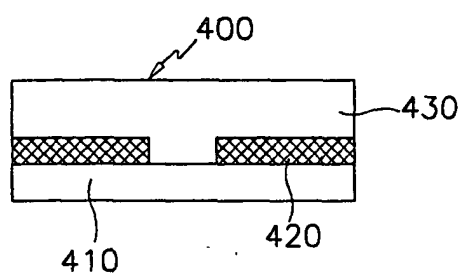


FIG.11

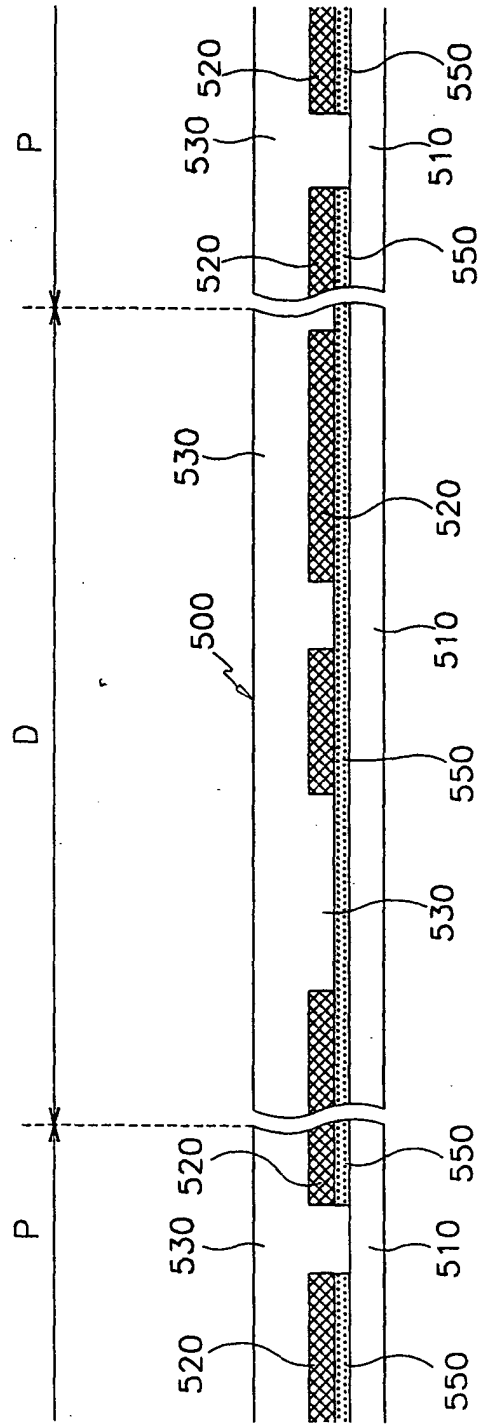


Figure 1 is a cross-sectional view of a multi-layered electronic device assembly. The assembly is built on a substrate 10. A central conductive layer 30 is formed on the substrate. Various components are mounted on the substrate, including a central block 70, side blocks 66, 62, and 64, and a top layer 55. A central vertical channel 40 is formed in the substrate. The assembly is divided into sections A, B, C, and D, with dimensions P, P', and D indicated. A central vertical line is labeled PR.

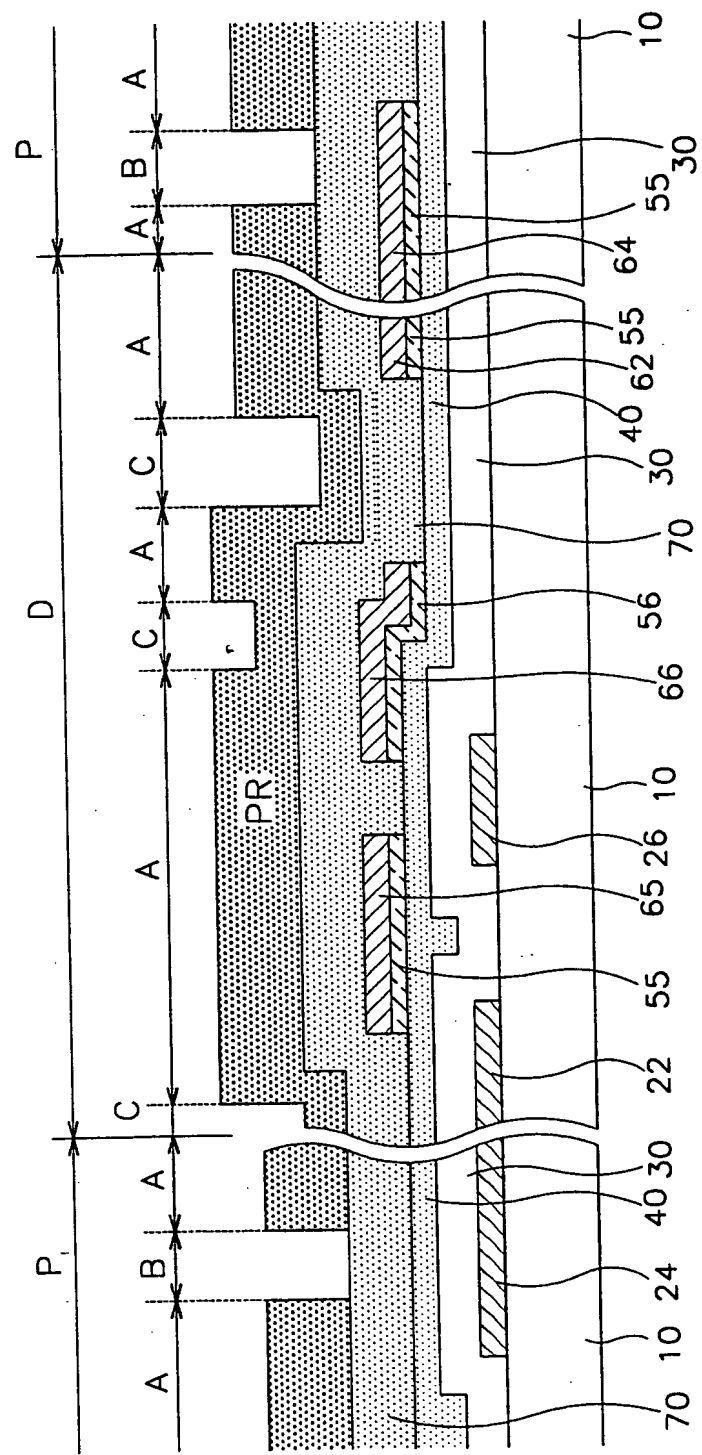


FIG. 12B

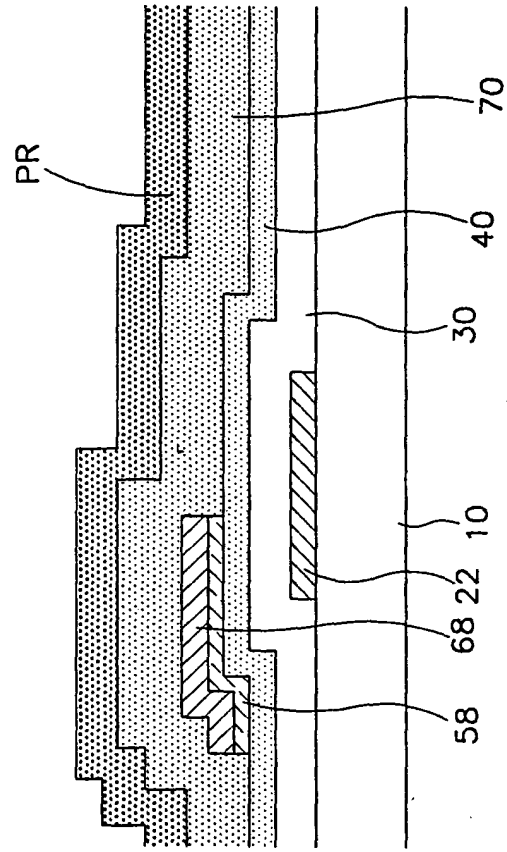


FIG. 13A

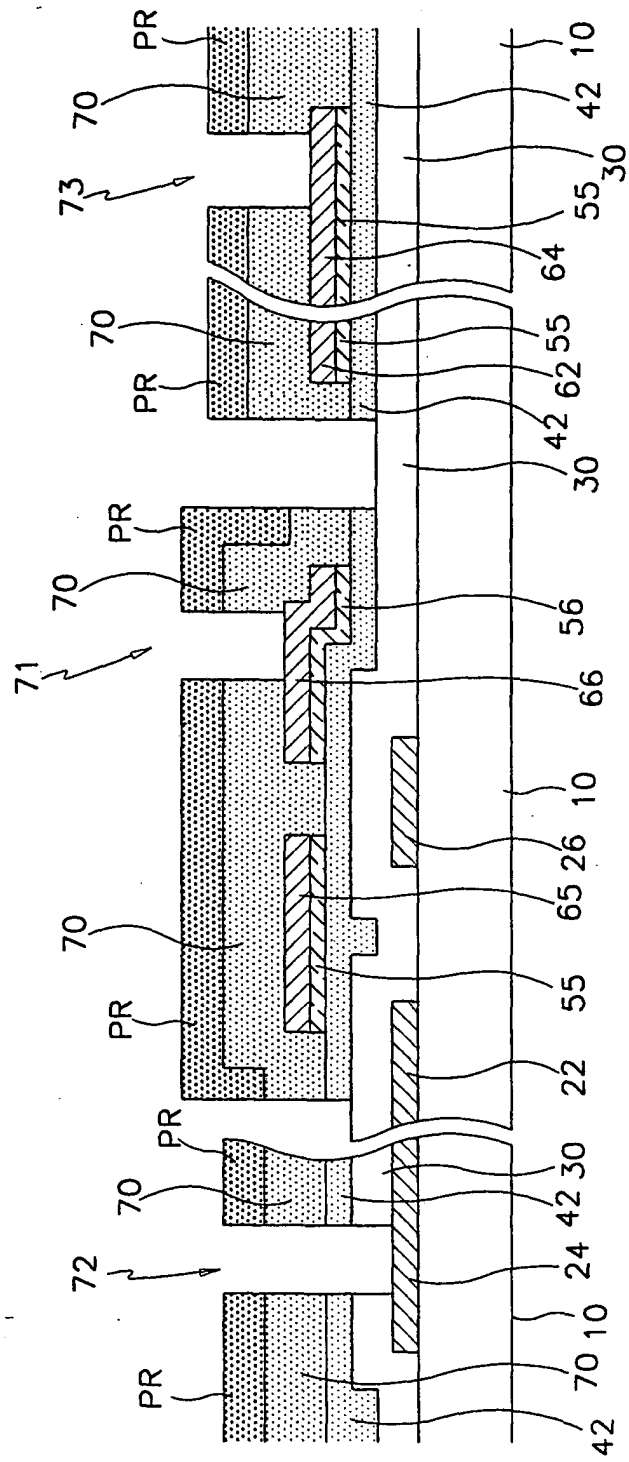
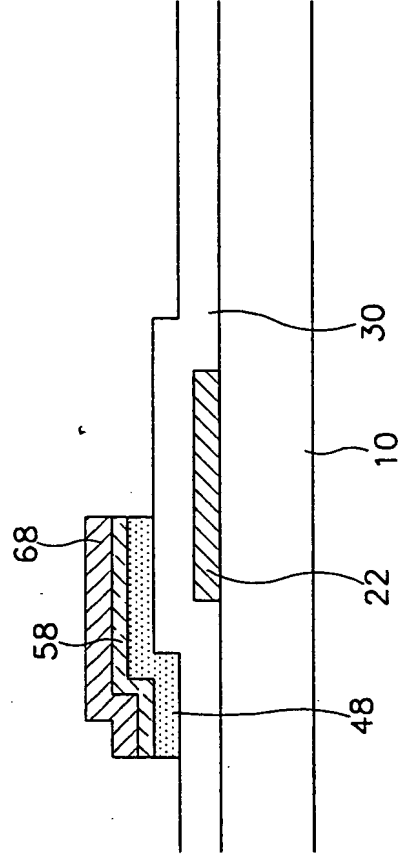


FIG. 13B



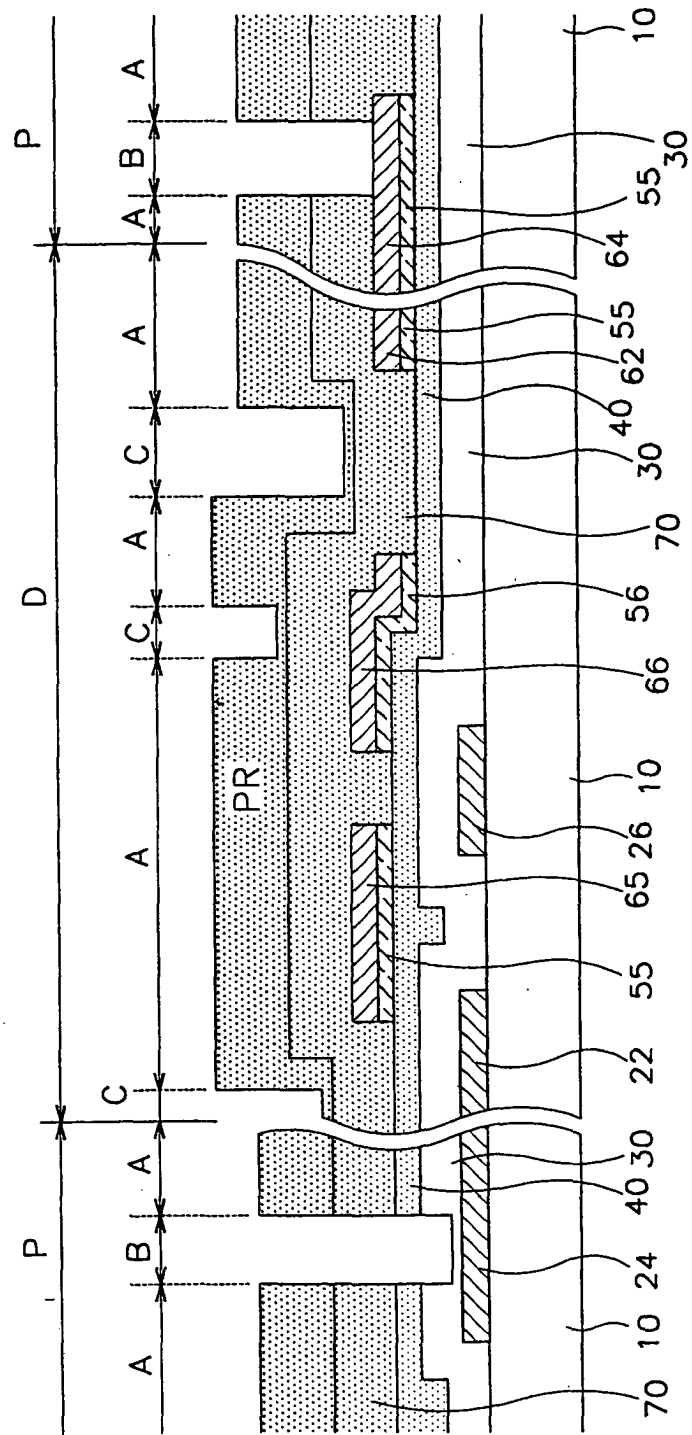


FIG. 14B

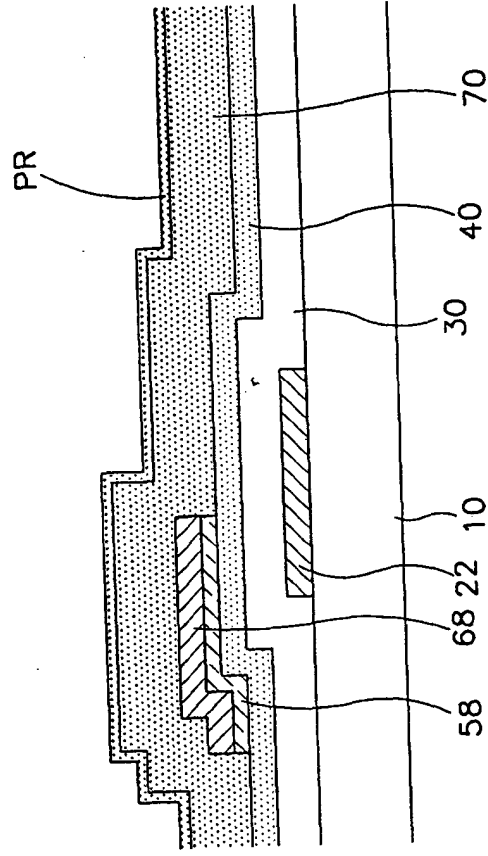


FIG. 15A

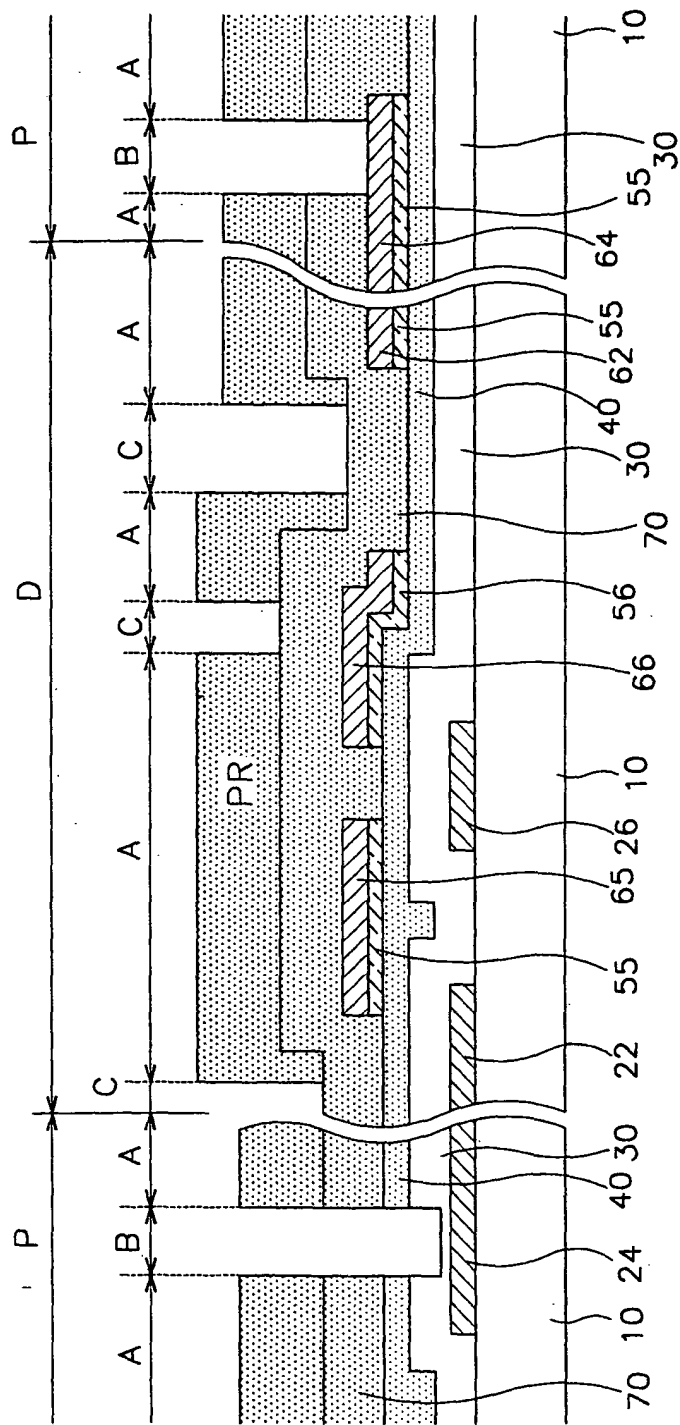


FIG.15B

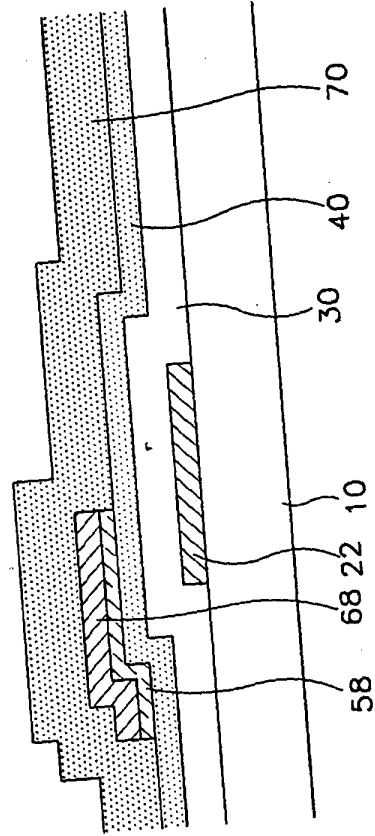


FIG. 16A

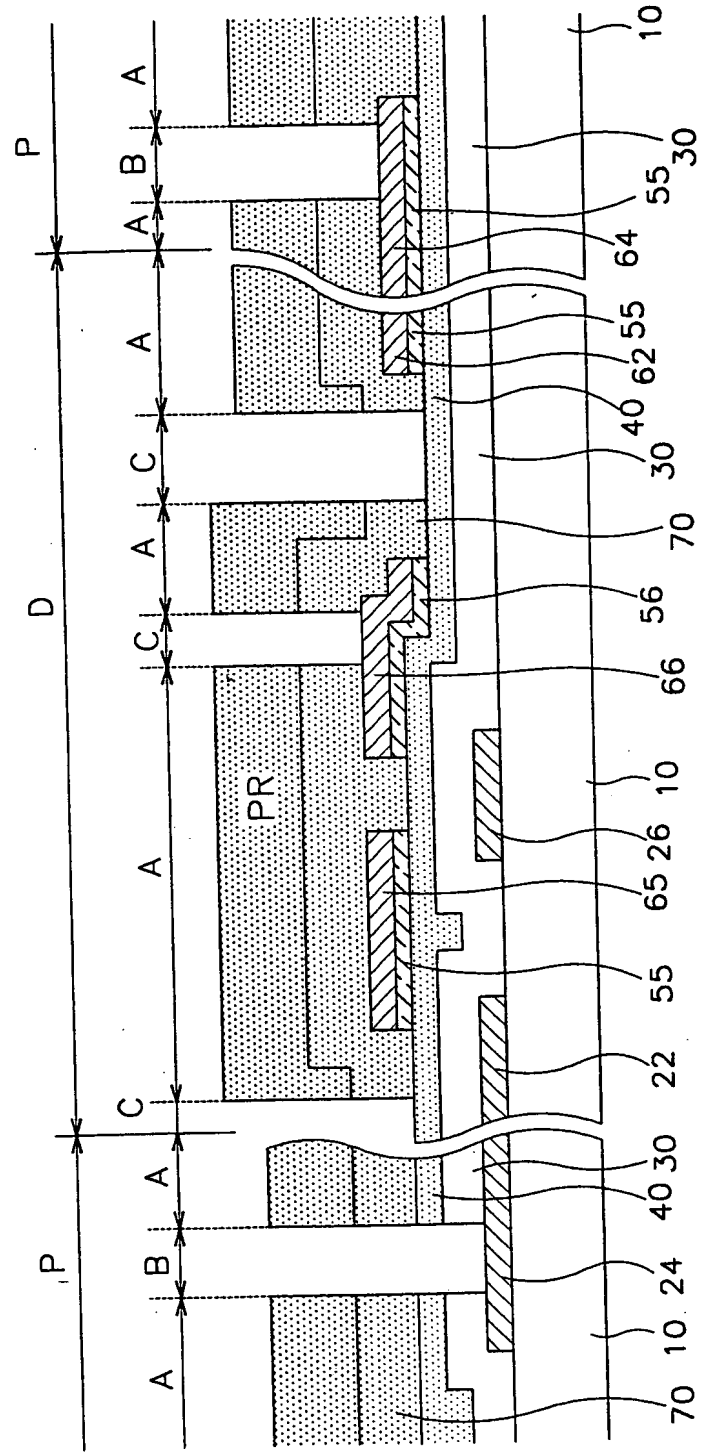


FIG. 16B

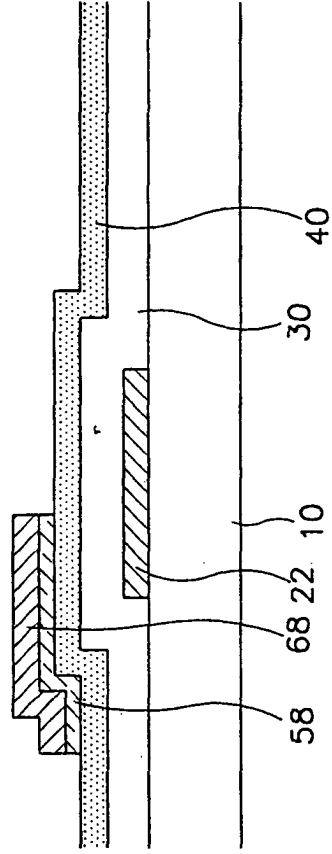


FIG.17A

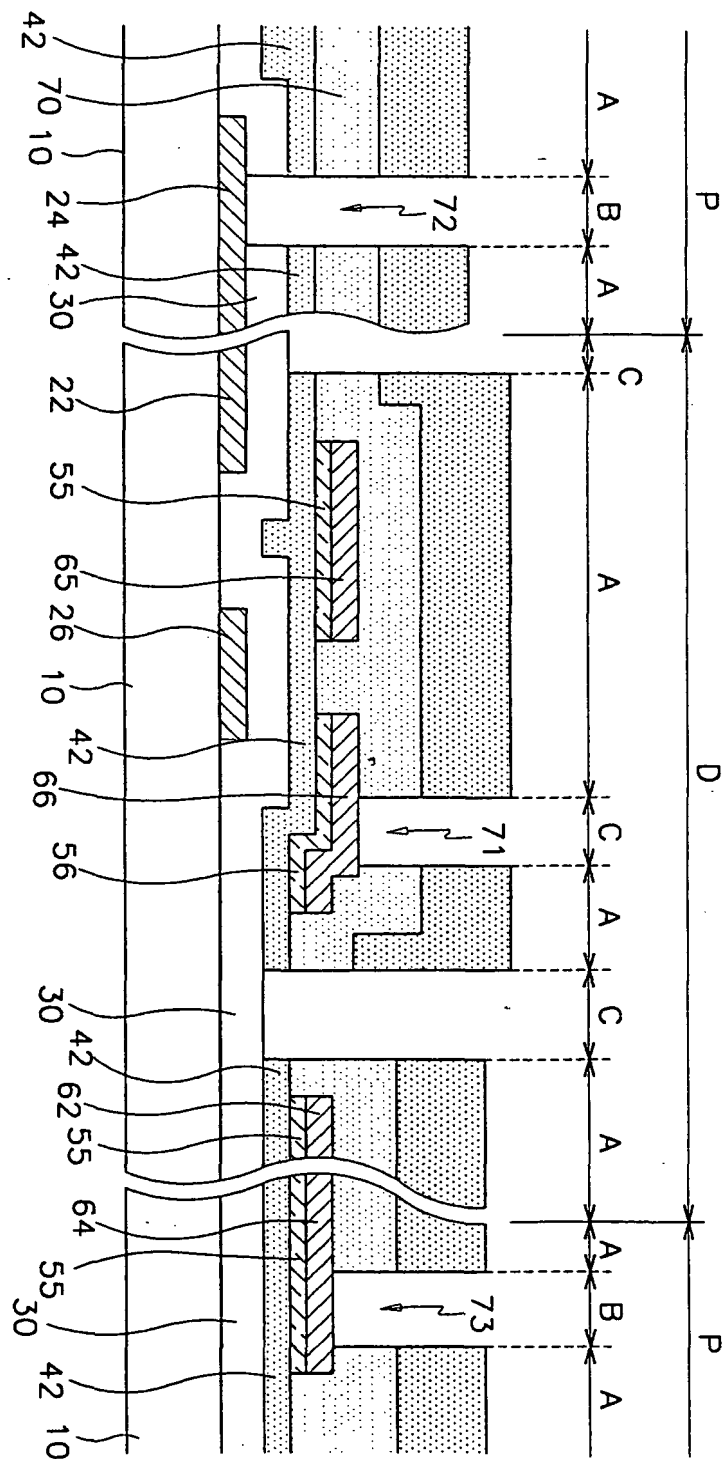


FIG. 17B

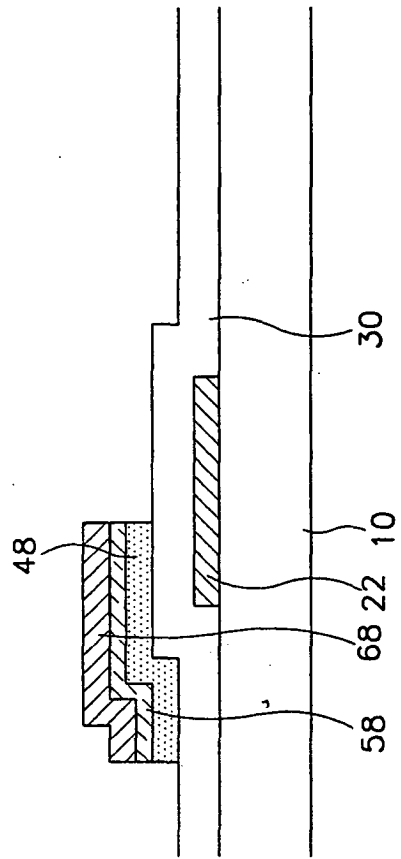


FIG. 19

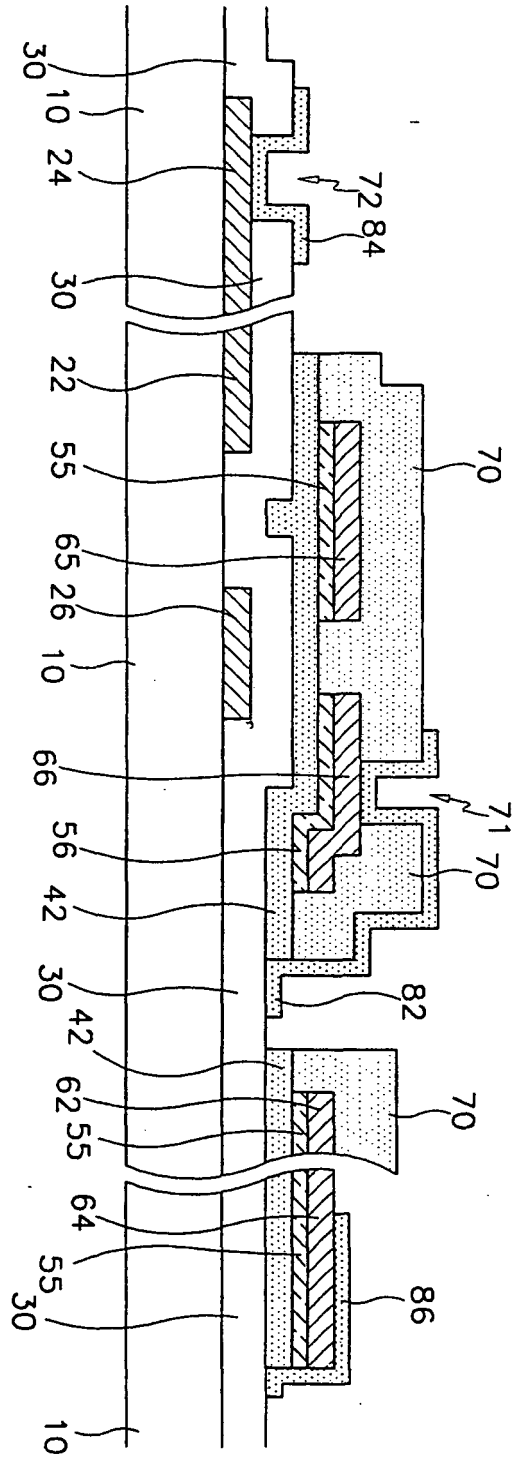


FIG.20A

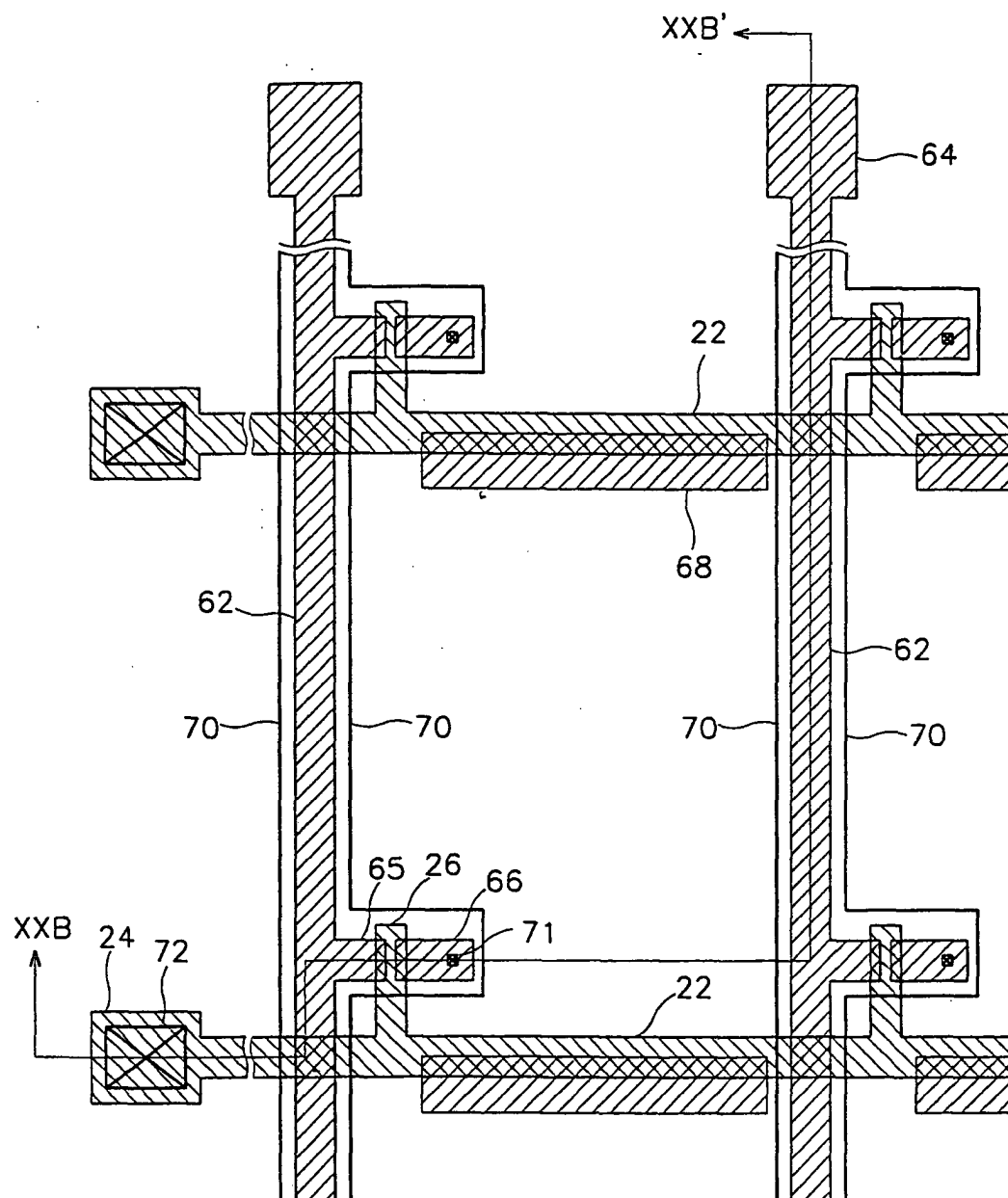


FIG.20B

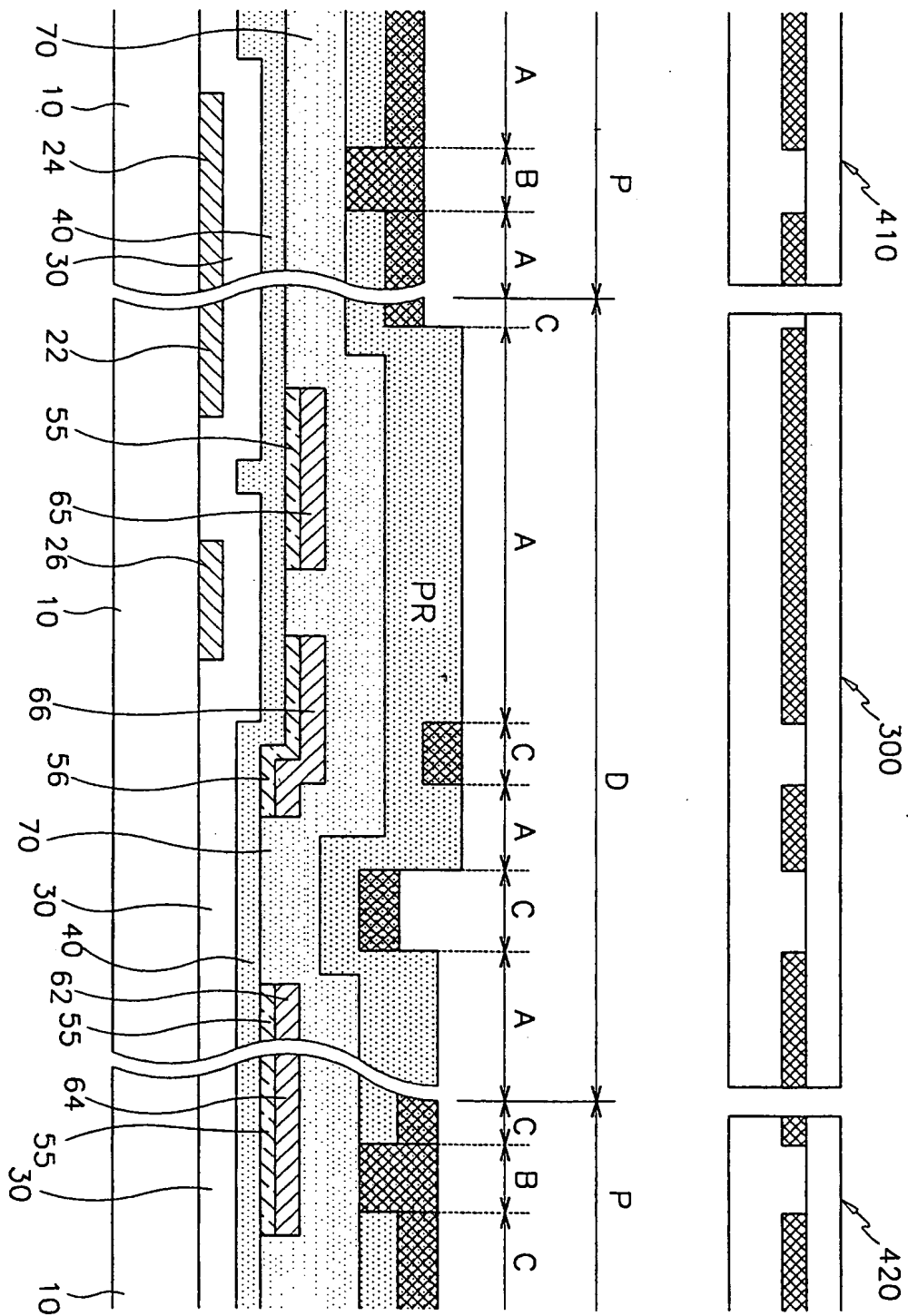


FIG.21

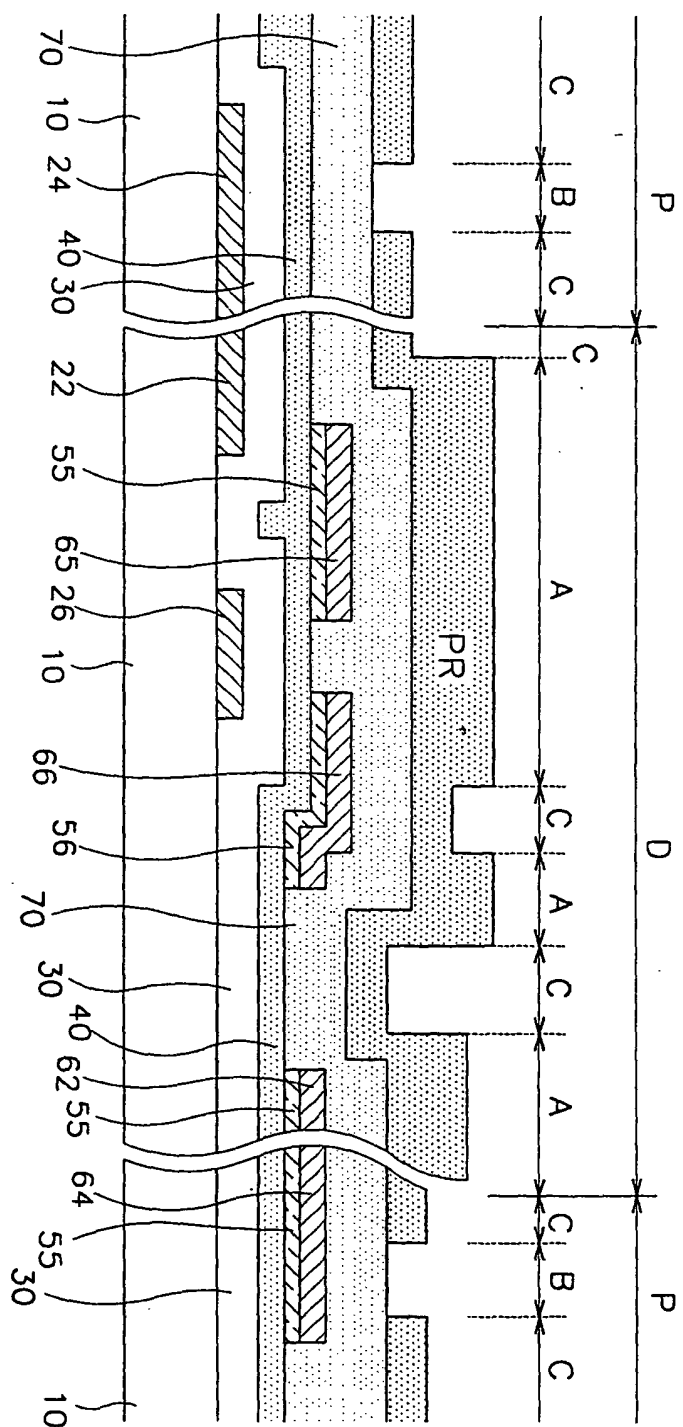


FIG.22

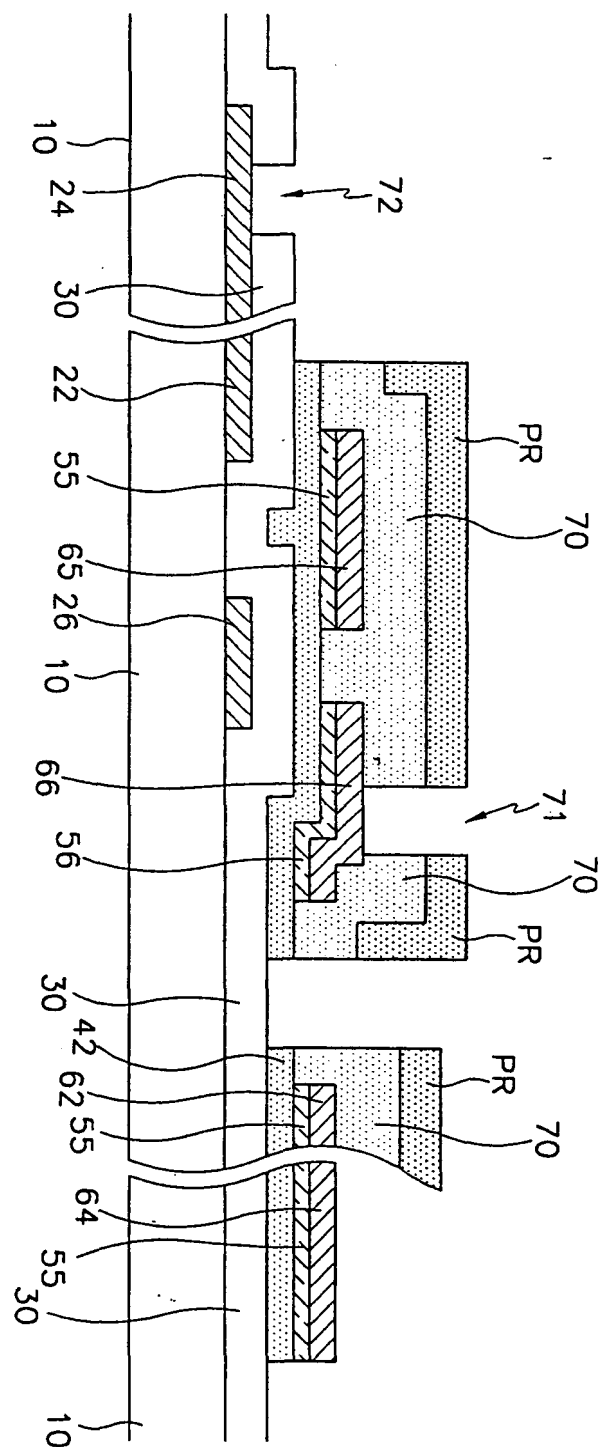


FIG.23A

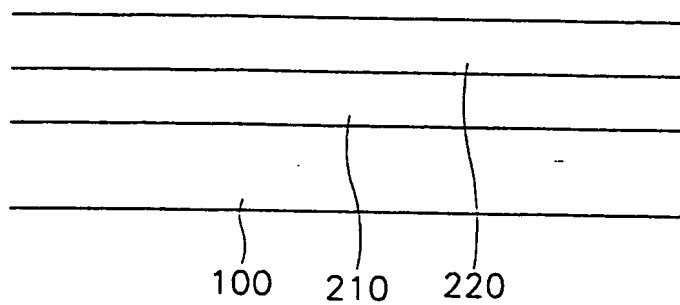


FIG.23B

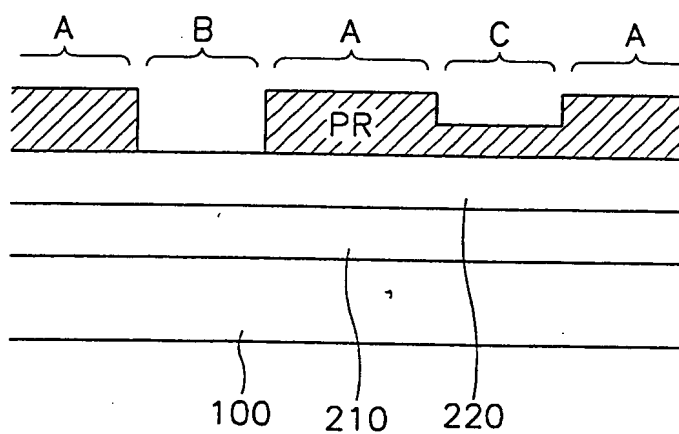


FIG.23C

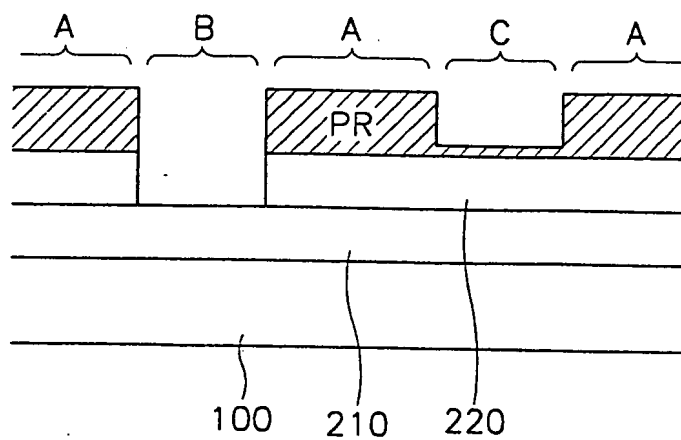


FIG.23D

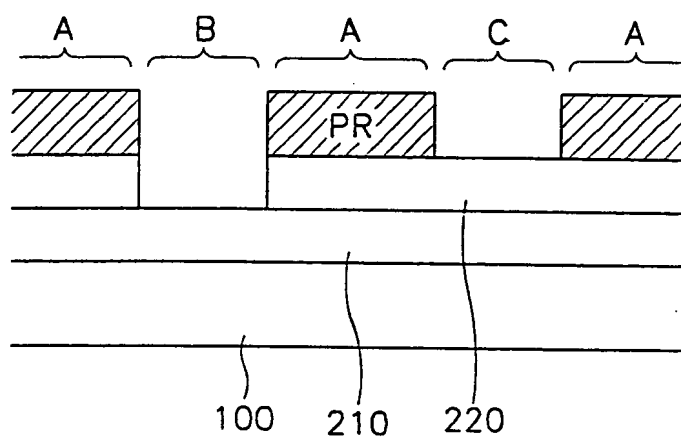


FIG.23E

